REMARKS

Claims 1-77 were allowed in this application. However, claims 40-51 have been cancelled in a prior amendment and claims 53, 54, 61, 62, 72 and 73 are being cancelled herein. Claims 2, 14, 19, 28, 32, 38, 39, 52, 58, 60, 65, 70, 71 and 77 have been amended. New dependent claims 78-81 have been added. These new claims are believed to be allowable since they depend from dependent claims and further in view of the features in these claims.

Paragraphs [0063] and [0071] have been amended to correct a typographical error and to provide the reference to the patent that issued from the published application referred to in the specification.

A number of references are made of record in a Supplemental Information Disclosure Statement that accompanies this amendment. The following are comments on one of these references in relation to the claims presently standing in this application:

US Patent Publication 2004/0105308 A1 and Claims 28, 52, 60 and 71

Claims 28, 52 and 71 have been amended to require that a voltage level at or about 0 volts and a positive voltage level be applied to at least two charge storage transistors in the string that is inhibited from being programmed between the selected word line and the source line. This has the advantage of suppressing breakdown mechanism(s) such as leakage and/or band-to-band tunneling while adequate to isolate the two boosted regions. See method 6 in the Table on page 23 and Paragraph [0061] of the present application. Such feature distinguishes the three claims over US Patent Publication 2004/0105308 A1 since Publication 2004/0105308 A1 does not teach or suggest such feature.

Claim 60 has been amended to require that a voltage level at or about 0 volts and a positive voltage level be applied to the set of transistors between the selected word line and the source line in the string that is inhibited from being programmed. See Paragraphs [0065], [0066], [0069] and [0071] of the present application. As explained in these paragraphs, this feature in claim 60 has advantages similar to those explained above for

claims 28, 52 and 71, and distinguishes over US Patent Publication 2004/0105308 A1 since Publication 2004/0105308 A1 does not teach or suggest such feature.

US Patent 5,715,194 (of record) and Claim 14

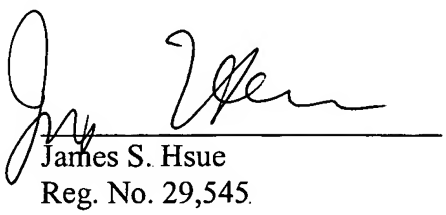
From Fig. 8 of the '194 patent, when transistor 104g' (which is 3 storage transistors away from the source line) is programmed, 2 volts is coupled to transistors 104j' and 104f' and 9 volts will be applied to word line 306d and coupled to transistor 104f". Therefore, the voltage (9V) coupled to the transistor 104f" adjacent to the select transistor is the same as that coupled to other transistors (e.g. 104k') in string 302b'. This will cause breakdown at the drain side of the select transistor in string 302a' addressed by word line 312'(SG_S), and may cause the charge state of the transistor in string 302a' addressed by word line 306d to change.

Claim 14 as amended differs from the '194 patent. In claim 14, the voltages are applied so that at least one of the two transistors programmed in sequence will be away from the source line by at least 3 charge storage transistors. When this happens, the voltage level coupled to the charge storage transistor adjacent to the one of the select transistors is different from those coupled to other transistors in the same string.

CONCLUSION

Claims 1-39, 52, 55-60 and 63-71 and 74-81 are presently pending in this application. This application is believed to be allowable as presented herewith and an early indication of allowability is earnestly solicited. However, if the Examiner is aware of any additional matters that should be discussed, a call to the undersigned attorney at: (415) 318-1162 would be appreciated.

Respectfully submitted,



James S. Hsue
Reg. No. 29,545

May 16, 2006
Date